Status of the EVM project

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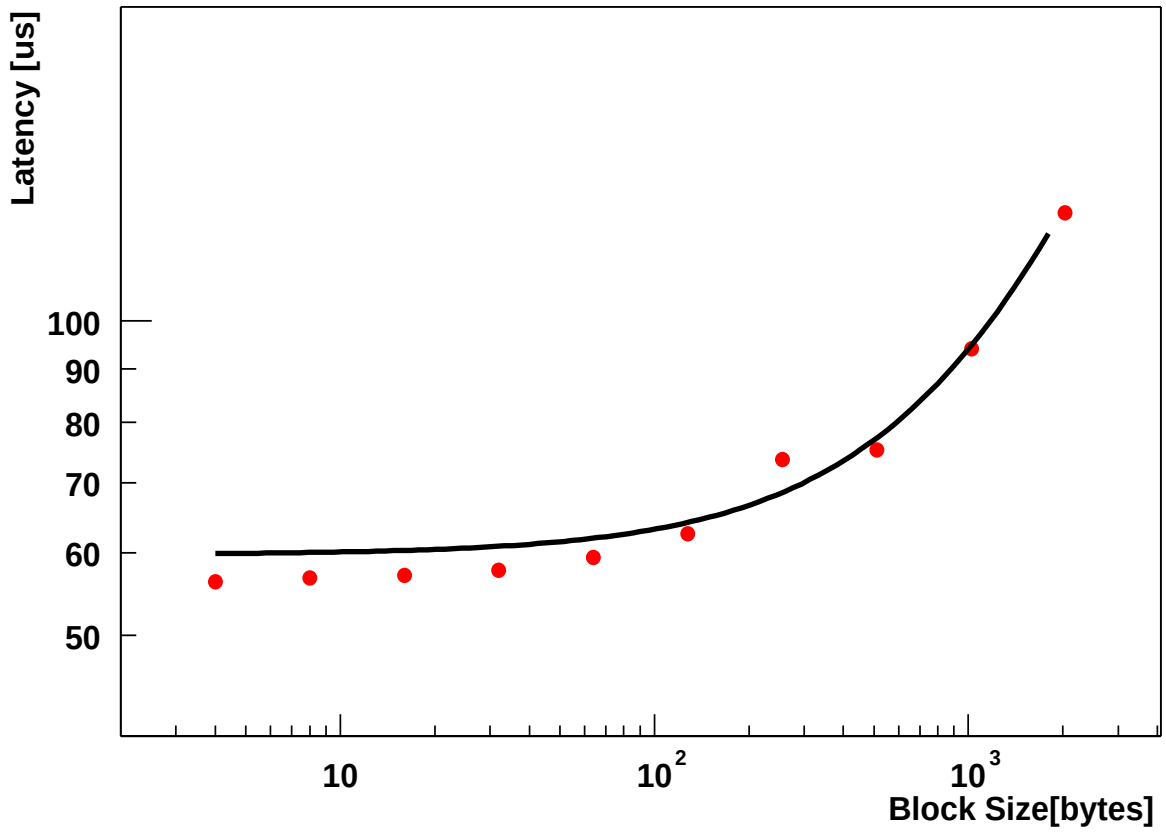
EVM test bench updates

- Four additional PC nodes (1+8 in total)
  - Myrinet (PCI64A), Fast-Ethernet (public + private, M-VIA + FAZE capable), IEEE1394
  - Ready to use in early Oct.
- VME PowerPC board (MVME2300)
  - RM development
  - IEEE1394 bus fan-out board development
- 50% of S. Aziz joined to the project

IEEE1394 benchmark (S.Pavlon)

- Linux kernel 2.2.14 + beta driver (20000616)
- Asynchronous write



IEEE1394 benchmark

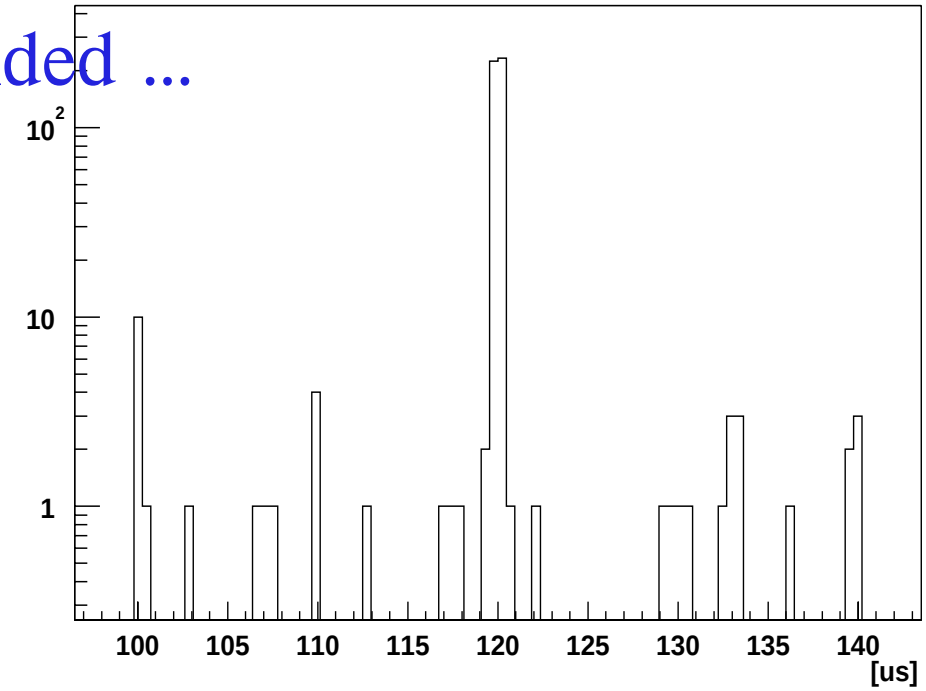
- Result on asyn. write transfer
  - Latency: 50μs
  - Bandwidth: 30MB/s
- User space host-to-host transfer
  - Code for polling packet receive was O.K.
  - Now, an application code transferring packet is under development

EVM software on XDAQ

- XDAQ BM is modified so that
  - it stores Evt-ID information in an object shared between BM and RM, and,
  - it keeps statistical information in ROOT
  - histograms and ntuples.
- The BM worked on cmslx and vxwcmsru.
- RM code is still under development. (original XDAQ RM is used in the test.)

EVM software on XDAQ

- Information kept in the BM:
  - Evt-ID life time
  - # of allocated Evt-IDs
  - ... to be expanded ...

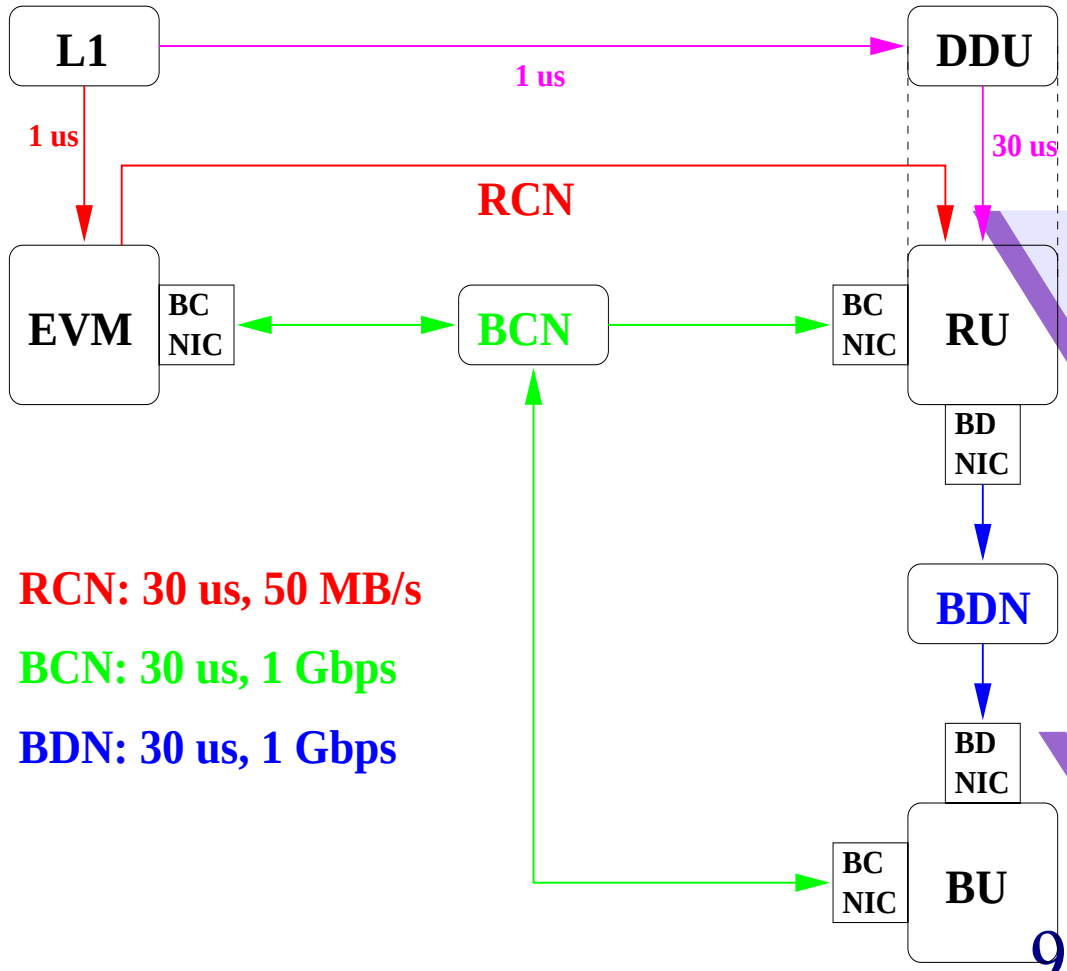


DAS Simulation (M.Litmaath)

- Lots of modifications / improvements
  - Separate BCN and BDN
  - Direct mode protocol (was indirect mode)
  - All control messages are packed by 100
  - Code clean-up
  - Stored in CVS under CMSDAQSIM/Fermilab
- Plan
  - Comparison of histograms with the test bench
  - Clean-up, documents ....

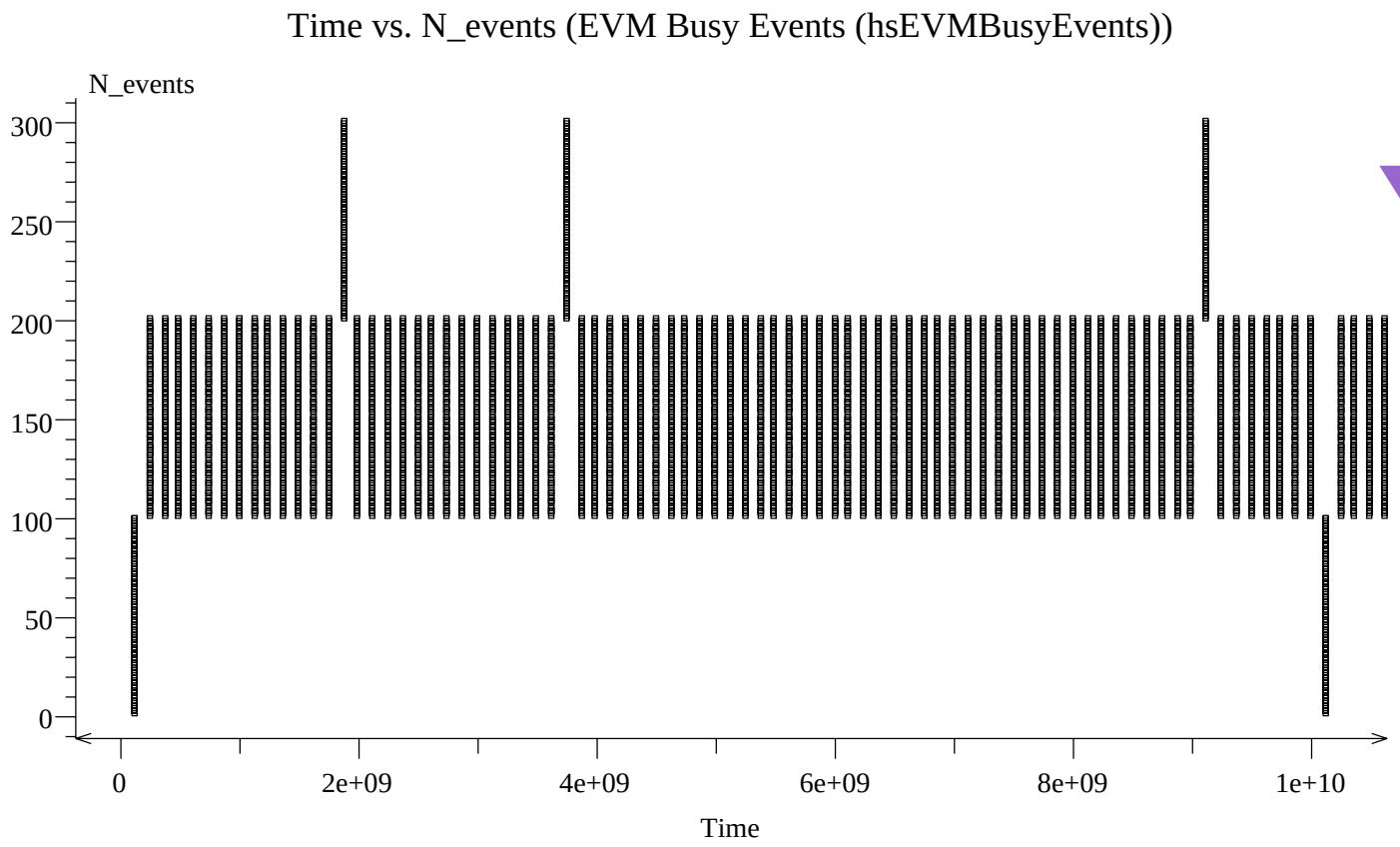
Simulator Setup

- 4 RUs, 4 BUs, 10 FUs/BU(500x500 was also done)
- L1: 800Hz
- L2: 1ms
- L3: 10ms



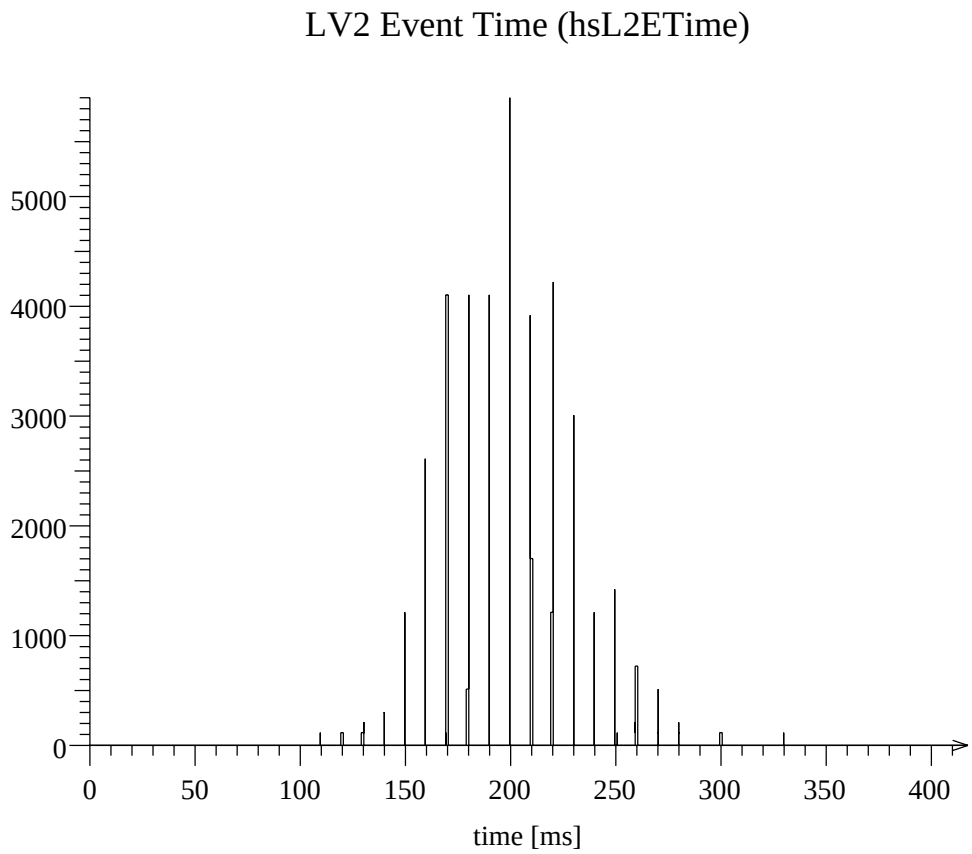
DAS Simulation

- # of allocated Evt-IDs



DAS Simulation

- Evt-ID life time



EVM development plan

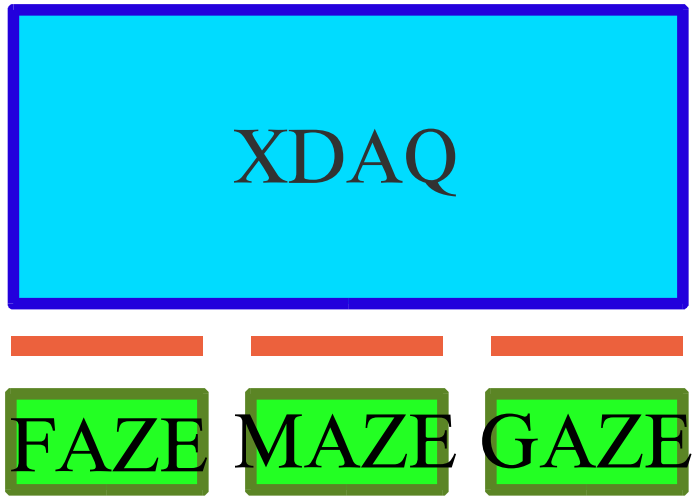
- Interoperability test
- RCN software development and benchmark
- IEEE1394 evaluation
- Simulator/test bench comparison
  - Improvement of the simulator
  - Studies on scalability
- Run control for XDAQ (C. Moore)

Summary

- FNAL EVM test bench is expanded for the further developments.
- Updated IEEE1394 benchmark shows reasonable bandwidth and latency.
- XDAQ based BM software is running.
- With updated simulator and XDAQ software, we are ready to compare simulation to the real system.

Interoperability

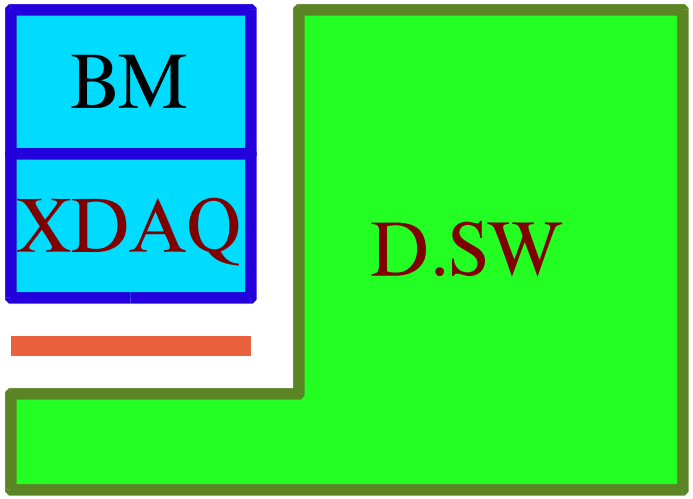
- XDAQ + special drivers



- We need ‘pt‘s for FAZE, MAZE....

Interoperability

- XDAQ-BM + Demonstrator Software



- We need TCP/IP transport of D.SW